ABSTRACT

A system, such as a complex computer system, incorporates several programmable logic devices coupled to load their configuration code from associated EEPROMs; typically this load is automatic on powerup. The EEPROMs connect to one of several serial busses, typically JTAG busses, connecting the EEPROMs with a common configuration logic. A processor is configured to write programmable logic configuration code from its memory through the common configuration logic and over the serial busses into the EEPROMs. The processor is also capable of connecting to a network and fetching configuration code for writing to the EEPROMs.